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| Standard Cells For Decimal Cirsuits |
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Standard Cells For Decimal Cirsuits

Prof. Hosam .A .Fahmi

**Abstract:**

The need for fast and powerful processors has called for the design of complicated standard cells that are capable of doing a lot of functions; one of these functions is the decimal computations that demand the design of fast standard cells to be able to design fast and powerful mathematical circuits.

The goal of our project is to design and simulate a decimal standard cells library, so that any designer can be able to use these cells to build a decimal circuits using VHDL code. There are two main goals to achieve in this project:

1. Design and simulation of fast standard cells for building decimal adders and multipliers.

2. Characterizing these standard cells so that different CAD tools can use them. We have done a standard cell for a one digit decimal adder and standard cells for decimal multiplier.

As we all know, the revolutionary progress that we live these days in all different fields of life has become the trait of this era. Mobiles and Computers have all become amazingly fast these days. For example, some processors nowadays can keep working up

to 4 or 5 GHz as a clock which is a very high speed compared to the speed that we had 4

years ago.

With this progress, we need fast devices that can cope with our daily needs. For many years, most of the Arithmetic Logic Units (ALU) - used in different processors - were based on binary arithmetic operations, it’s not until very recently that the need for decimal circuits arose. Specially, in the financial, commercial, and industrial computing, where subtle conversion and rounding errors that are inherent to floating point binary representations cannot be tolerated. From this two aspects, the idea of our project came out, Standard Cells for Decimal Circuits. The goal of our project is to design standard cells for decimal circuits like adders and multipliers, so that the designer can find a library that helps him in making an efficient, area-delay optimized decimal circuits.

We are required to design fast basic building blocks, which can be used in building bigger decimal circuits such as 16-digit adder or multiplier. These basic blocks need to be area-delay optimized for fast operation, layout designed using CAD tools using a full custom approach (to minimize the delay as much as possible), tested for proper operation after designing the layout, then finally, characterized with the delay and capacitance of each cell, so that any HDL complier can use them correctly.

The output of our project is educational in the first place, we ought to learn using different CAD tools that are used in this field of industry, have a look at the state-of- the-art proposals in the decimal circuits topic, and finally, bringing out a library of these standard cells.